REMARKS

Claims 1-7 stand rejected as obvious over U.S. Patent No. 5,959,442 ("Hallberg") in view of U.S. Patent No. 5,777,383 ("Stager"). Claims 8-45 stand rejected as obvious over Hallberg and Stager in combination with U.S. Patent No. 4,074,342 ("Honn").

Claim 1 calls for a flip-chip type integrated circuit chip that includes a power switch to alternately couple and decouple the input terminal to the output terminal. The chip includes a p-type region and an n-type region, and the first power switch includes a plurality of p+ regions fabricated in the n-type region in a first array, and a plurality of n+ regions fabricated in the p-type region in a second array, and wherein alternating p+ regions are connected to the input terminal and to an intermediate terminal, and alternating n+ regions chip are connected to the intermediate terminal and to ground.

Claim 27 calls for a substrate having a first plurality of doped regions and a second plurality of doped regions and an array of metalized pads fabricated on a surface of the substrate. The first and second pluralities of doped regions are arranged in a first alternating pattern. The array of pads includes a first plurality of pads and a second plurality of pads, with the first and second pluralities of pads arranged in a second alternating pattern. The first plurality of pads are electrically connected to the first plurality of doped regions, the second plurality of pads are electrically connected to the second plurality of doped regions, the first plurality of pads are connected to a first terminal of the voltage regulator, and the second plurality of pads are connected to a second terminal in the voltage regulator.

Claim 36 calls for a PMOS switch fabricated on a chip with a first alternating pattern of source pads and drain pads, an NMOS switch fabricated on the chip with a second alternating pattern of source pads and drain pads, and a substrate having a first electrode to electrically couple the drain pads of the PMOS and NMOS switches to an intermediate terminal, a second electrode to electrically couple the source pads of the PMOS switch to the input terminal, a third electrode to electrically couple the source pads of the NMOS switch to ground.

Claim 44 calls for a chip having an array of pads formed thereon and a substrate having a signal layer formed thereon with a first electrode and a second electrode. Each pad is connected to a plurality of doped regions to create a distributed array of transistors. The first electrode has

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a body and a plurality of fingers that extend from the body toward the second electrode, the second electrode has a body and plurality of fingers that extend toward the first electrode, and the fingers of the first electrode and are interdigited with the fingers of the second electrode and each finger overlies and is electrically coupled to a row of pads on the chip.

Hallberg, Stager and Honn do not teach or suggest the various limitations relating to the layout of the doped regions and pads and their connections to the terminals. For example, Hallberg, Stager and Honn do not teach doped regions in an array with alternating regions of the array connected to different terminals, an array of pads with two pluralities of pads arranged in an alternating pattern and electrically connected to two doped regions, or two electrodes having interdigited fingers.

Applicant submits that the claims are in condition for allowance, which action is requested. Filed herewith is a Petition for Automatic Extension with the required fee.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12/13/00

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